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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,316	KARASAWA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,13,14,17 and 18* is/are rejected.

7)☒ Claim(s) *7,11,12 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The present Office Action is supplement to the Office Action mailed on 12/4/03.

2. Claim 15 is objected to because of the following informalities: lines 1-2, the phrase "the second conductive layer" has no antecedent basis. Appropriate correction is required.

3. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification (figs. 1 and 3) discloses the first gate-gate electrode layer [20] and the first drain-gate wiring layer [30] are formed by a first single conductive layer. The specification (figs. 1 and 3) discloses the second gate-gate electrode layer is formed by a second single conductive layer [22]. Therefore, it is unclear how the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer as claimed in claim 13. It is believed that the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer level.

The specification (figs. 1 and 4) discloses the first drain-drain wiring layer [40] is formed by a first single conductive layer. The second drain-drain wiring layer [42] is formed by a second single conductive layer. The lower layer [32a] is formed by a third single conductive layer. Therefore, it is unclear how the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer as claimed in claim 13. It is believed that the first drain-drain wiring layer, the

second drain-drain wiring layer and the lower layer are located in a second conductive layer level.

Since there are first and second conductive layer levels, it is believed that the upper layer is located in a third conductive layer level.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Song.

In regards to claim 1, Song shows all the elements of the claimed invention in figs. 2-13. It is a semiconductor device provided with a memory cell including a first driver transistor TD1, a second driver transistor TD2, a first transfer transistor TA1, a second transfer transistor TA2, a first load transistor TL1 and a second load transistor TL2. The semiconductor transistor comprising: a first gate-gate electrode layer [5a] including a gate electrode of the first load transistor TL1 and a gate electrode of the first driver transistor TD1; a second gate-gate electrode layer [5b] including a gate electrode of the second load transistor TL2 and a gate electrode of the second driver transistor TD2; a first drain-drain wiring layer [9i'] which forms a part of a connection layer that electrically connects a drain region LD1 of the first load transistor TL1 and a drain region DD1 of

the first driver transistor TD1; a second drain-drain wiring layer [9i"] which forms a part of a connection layer that electrically connects a drain region LD2 of the second load transistor TL2 and a drain region DD2 of the second driver transistor TD2; a first drain-gate wiring layer [9i"] which forms a part of a connection layer that electrically connects the first gate-gate electrode layer [5a] and the second drain-drain wiring layer [9i"]; a second drain-gate wiring layer [9i'] which forms a part of a connection layer that electrically connects the second gate-gate electrode layer [5b] and the first drain-drain wiring layer [9i']; and a first active region LD1 in which the first load transistor TL1 is provided, wherein the first drain-gate wiring layer [9i"] and the second drain-gate wiring layer [9i'] are located in different layers, respectively (fig. 5), and wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region LD1 (fig. 3).

In regards to claim 2, Song further discloses the first protruded active region LD1 is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [TD1, TD2] are provided.

In regards to claim 3, Song further discloses a part of the first active region and the first protruded active region form an L-shape.

In regards to claim 4, Song further discloses a second active region LD2 in which the second load transistor TL2 is provided; and a second protruded active region provided in a manner to protrude from an end portion of the second active region.

In regards to claim 5, Song further discloses the second protruded active region LD2 is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [TD1, TD2] are provided.

In regards to claim 6, Song further discloses a part of the second active region and the second protruded active region form an L-shape.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song.

Song (col. 1, line 15 to col. 2, line 5) discloses a memory system (cache memory devices) can be made of a CMOS SRAM.

Song differs from the claimed invention by now showing a CMOS SRAM defined in any one of claims 1-6.

Song (figs. 2-13) discloses a CMOS SRAM defined in any one of claims 1-6.

Since Song discloses a CMOS SRAM used as a memory element, it would have been obvious to have the CMOS SRAM (figs. 2-13) of Song in the memory system of Song because it improves the operating speed of the SRAM.

Song (col. 1, line 15 to col. 2, line 5) discloses an electronic apparatus (computers) can be made of a CMOS SRAM.

Song differs from the claimed invention by now showing a CMOS SRAM defined in any one of claims 1-6.

Song (figs. 2-13) discloses a CMOS SRAM defined in any one of claims 1-6.

Since Song discloses a CMOS SRAM used as a memory element, it would have been obvious to have the CMOS SRAM (figs. 2-13) of Song in the computer of Song because it improves the operating speed of the SRAM.

8. Claims 1-6, 8-10, 17 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Komori.

In regards to claim 1, Komori shows all the elements of the claimed invention in figs. 39-41. It is a semiconductor device provided with a memory cell including a first driver transistor [101], a second driver transistor [104], a first transfer transistor [103], a second transfer transistor [106], a first load transistor [102] and a second load transistor [105]. The semiconductor transistor comprising: a first gate-gate electrode layer [111] including a gate electrode of the first load transistor [102] and a gate electrode of the first driver transistor [101]; a second gate-gate electrode layer [112] including a gate electrode of the second load transistor [105] and a gate electrode of the second driver transistor [104]; a first drain-drain wiring layer [116] which forms a part of a connection layer that electrically connects a drain region of the first load transistor [102] and a drain region of the first driver transistor [101]; a second drain-drain wiring layer [115] which forms a part of a connection layer that electrically connects a drain region of the second load transistor [105] and a drain region of the second driver transistor [104]; a first drain-gate wiring layer [111] which forms a part of a connection layer that electrically connects

the first gate-gate electrode layer [111] and the second drain-drain wiring layer [115]; a second drain-gate wiring layer [116] which forms a part of a connection layer that electrically connects the second gate-gate electrode layer [112] and the first drain-drain wiring layer [116]; and a first active region [140] in which the first load transistor [102] is provided, wherein the first drain-gate wiring layer [111] and the second drain-gate wiring layer [116] are located in different layers, respectively, and wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

In regards to claim 2, Komori further discloses the first protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [101, 104] are provided.

In regards to claim 3, Komori further discloses a part of the first active region [140] and the first protruded active region form an L-shape.

In regards to claim 4, Komori further discloses a second active region [160] in which the second load transistor [105] is provided; and a second protruded active region provided in a manner to protrude from an end portion of the second active region.

In regards to claim 5, Komori further discloses the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [101, 104] are provided.

In regards to claim 6, Komori further discloses a part of the second active region and the second protruded active region form an L-shape.

In regards to claim 8, Komori further discloses the first drain-gate wiring layer [111] is located in a layer lower than the second drain-gate wiring layer [116].

In regards to claim 9, Komori further discloses the first drain-gate wiring layer [111] is located in a layer in which the first gate-gate electrode layer [111] is provided.

In regards to claim 10, Komori further discloses the second drain-gate wiring layer [116] is formed across a plurality of layers [111, 115].

In regards to claim 17, Komori further discloses a memory system (SRAMs) provided with the semiconductor device defined in any of claims 1-6 and 8-10 (col. 1, line 13 to col. 3, line 19).

In regards to claim 18, Komori further discloses an electronic apparatus (a semiconductor device of portable apparatus) provided with the semiconductor device defined in any one of claims 1-6 and 8-10 (col. 1, line 13 to col. 3, line 19).

9. Claims 7 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is the second drain-gate wiring layer is electrically connected to the first drain-drain wiring layer through a contact section. The second major difference in the claims not found in the prior art of record is the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer,

and the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
January 12, 2004

Primary Examiner
Steven Loke